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February 2000

National Semiconductor

Jameco Part Number 51027

DS75451/2/3
Series Dual Peripheral Drivers

General Description

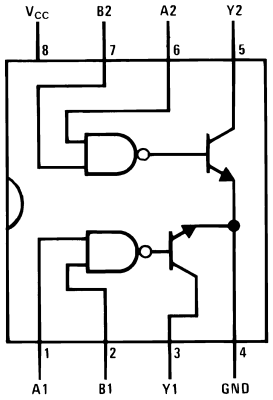
The DS7545X series of dual peripheral drivers is a family of versatile devices designed for use in systems that use TTL logic. Typical applications include high speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, bus drivers and memory drivers.

The DS75451, DS75452 and DS75453 are dual peripheral AND, NAND and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

Features

- 300 mA output current capability
- High voltage outputs
- No output latch-up at 20V
- High speed switching
- Choice of logic function
- TTL compatible diode-clamped inputs
- Standard supply voltages
- Replaces TI “A” and “B” series

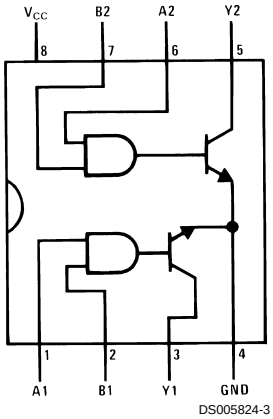
Connection Diagrams (Dual-In-Line and Metal Can Packages)



DS005824-2

*See (Note 5) and Appendix E regarding S.O. package power dissipation constraints.

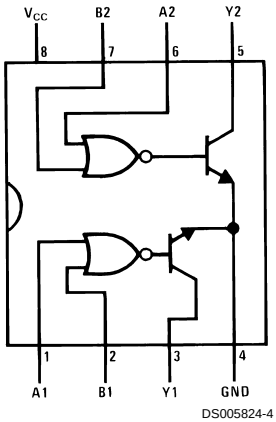
Top View
Order Number DS75451M or DS75451N



DS005824-3

Top View
Order Number DS75452M or DS75452N

See NS Package Numbers M08A* or N08E



DS005824-4

*See (Note 5) and Appendix E regarding S.O. package power dissipation constraints.

Top View
Order Number DS75453M or DS75453N

See NS Package Numbers M08A* or N08E

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, (V_{CC}) (Note 2)	7.0V
Input Voltage	5.5V
Inter-Emitter Voltage (Note 3)	5.5V
Output Voltage (Note 4)	30V
Output Current (Note 5)	300 mA
Maximum Power (Note 5) Dissipation† at 25˚C	
Molded DIP Package	957 mW
SO Package	632 mW
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering, 4 sec.)	260˚C

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})	4.75	5.25	V
Temperature, (T_A)	0	+70	˚C

†Derate molded package 7.7 mW/˚C above 25˚C, derate SO package 7.56 mW/˚C above 25˚C.

Electrical Characteristics

(Notes 6, 7)

Symbol	Parameter	Conditions				Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	(*Figure 7*)				2			V
V_{IL}	Low-Level Input Voltage							0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA						−1.5	V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, (*Figure 7*)	V_{IL} = 0.8V	I_{OL} = 100 mA	DS75451, DS75453		0.25	0.4	V
				I_{OL} = 300 mA	DS75451, DS75453		0.5	0.7	V
			V_{IH} = 2V	I_{OL} = 100 mA	DS75452		0.25	0.4	V
				I_{OL} = 300 mA	DS75452		0.5	0.7	V
I_{OH}	High-Level Output Current	V_{CC} = Min, (*Figure 7*)	V_{OH} = 30V	V_{IH} = 2V	DS75451, DS75453			100	µA
				V_{IL} = 0.8V	DS75452			100	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, (*Figure 9*)						1	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.4V, (*Figure 9*)						40	µA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.4V, (*Figure 8*)					−1	−1.6	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = Max, (*Figure 10*)	V_I = 5V		DS75451		7	11	mA
			V_I = 0V		DS75452		11	14	mA
			V_I = 5V		DS75453		8	11	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = Max, (*Figure 10*)	V_I = 0V		DS75451		52	65	mA
			V_I = 5V		DS75452		56	71	mA
			V_I = 0V		DS75453		54	68	mA

Switching Characteristics

(V_{CC} = 5V, T_A = 25˚C)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF, R_L = 50Ω, I_O ≈ 200 mA, (*Figure 14*)	DS75451		18	25	ns
			DS75452		26	35	ns
			DS75453		18	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF, R_L = 50Ω, I_O ≈ 200 mA, (*Figure 14*)	DS75451		18	25	ns
			DS75452		24	35	ns
			DS75453		16	25	ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 15 pF, R_L = 50Ω, I_O ≈ 200 mA, (*Figure 14*)			5	8	ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 15 pF, R_L = 50Ω, I_O ≈ 200 mA, *(Figure 14)*			7	12	ns

Switching Characteristics (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	High-Level Output Voltage after Switching	V_S = 20V, $I_O \approx$ 300 mA, (*Figure 15*)		V_S − 6.5			mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: The voltage between two emitters of a multiple-emitter transistor.

Note 4: The maximum voltage which should be applied to any output when it is in the "OFF" state.

Note 5: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 6: Unless otherwise specified min/max limits apply across 0˚C to +70˚C range. All typicals are given for V_{CC} = +5V and T_A = 25˚C.

Note 7: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Truth Tables (H = high level, L = low level)

DS75451

A	B	Y
L	L	L (ON State)
L	H	L (ON State)
H	L	L (ON State)
H	H	H (OFF State)

DS75452

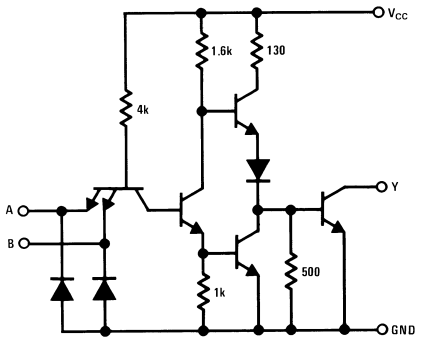
A	B	Y
L	L	H (OFF State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	L (ON State)

DS75453

A	B	Y
L	L	L (ON State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	H (OFF State)

Schematic Diagrams

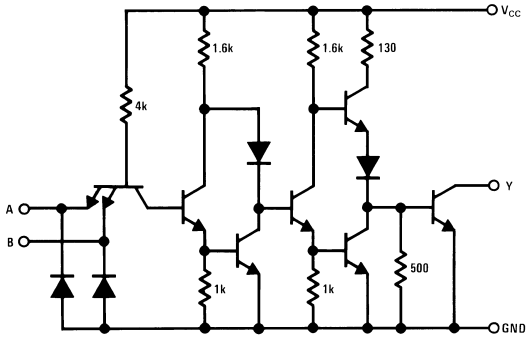
DS75451



DS005824-11

Resistor values shown are nominal.

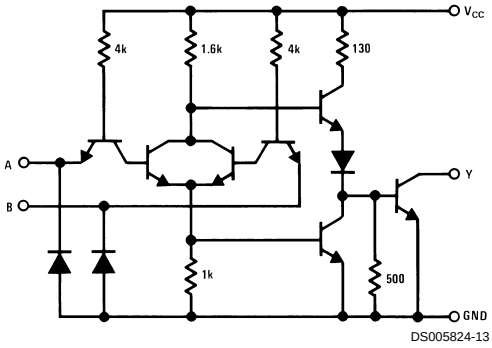
DS75452



DS005824-12

Resistor values shown are nominal.

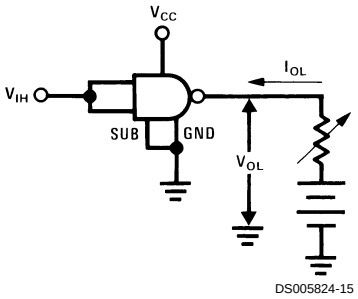
DS75453



DS005824-13

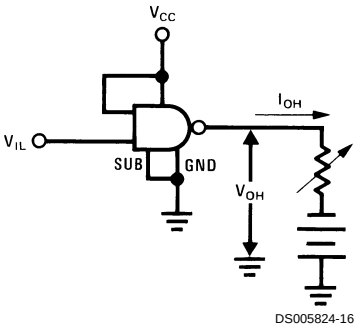
Resistor values shown are nominal.

DC Test Circuits



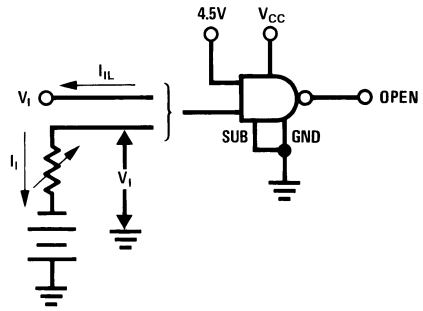
Both inputs is tested simultaneously.

FIGURE 1. V_{IH}, V_{OL}



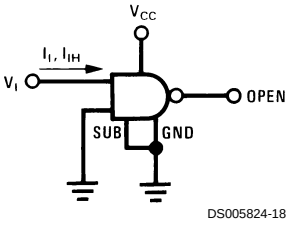
Each input is tested separately.

FIGURE 2. V_{IL}, V_{OH}



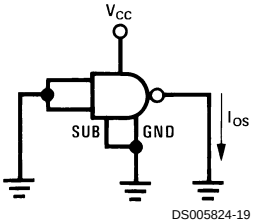
Each input is tested separately.

FIGURE 3. V_I, I_{IL}



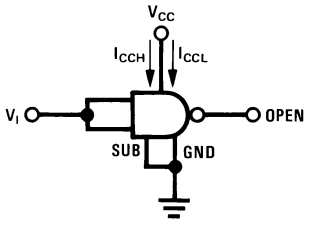
Each input is tested separately.

FIGURE 4. I_I, I_{IH}



Each input is tested separately.

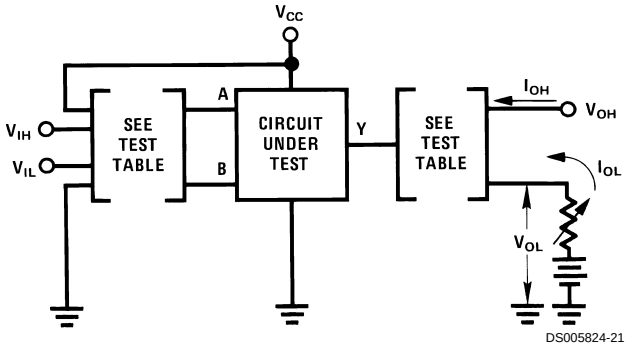
FIGURE 5. I_{OS}



Both gates are tested simultaneously.

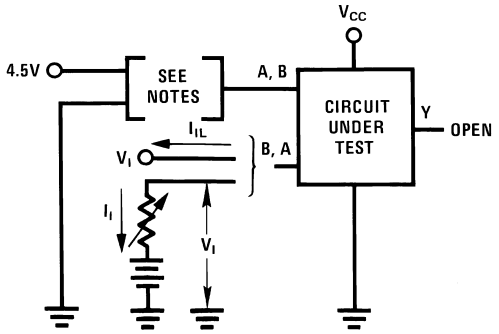
FIGURE 6. I_{CCH}, I_{CCL}

DC Test Circuits (Continued)



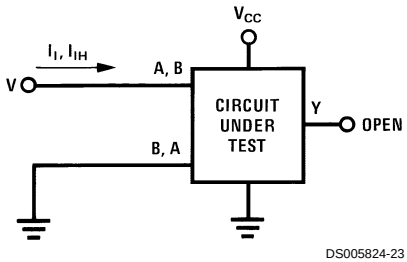
Circuit	Input Under Test	Other Input	Output	
			Apply	Measure
DS75451	V_{IH}	V_{IH}	V_{OH}	I_{OL}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
DS75452	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	V_{OH}	I_{OH}
DS75453	V_{IH}	Gnd	V_{OH}	I_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OH}

FIGURE 7. V_{IH}, V_{IL}, I_{OH}, V_{OL}



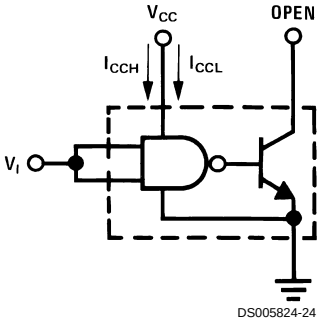
Note A: Each input is tested separately.
Note B: When testing DS75453 input not under test is grounded. For all other circuits it is at 4.5V.

FIGURE 8. V_I, V_{IL}



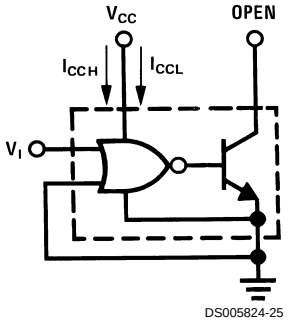
Each input is tested separately.

FIGURE 9. I_I, I_{IH}



Both gates are tested simultaneously.

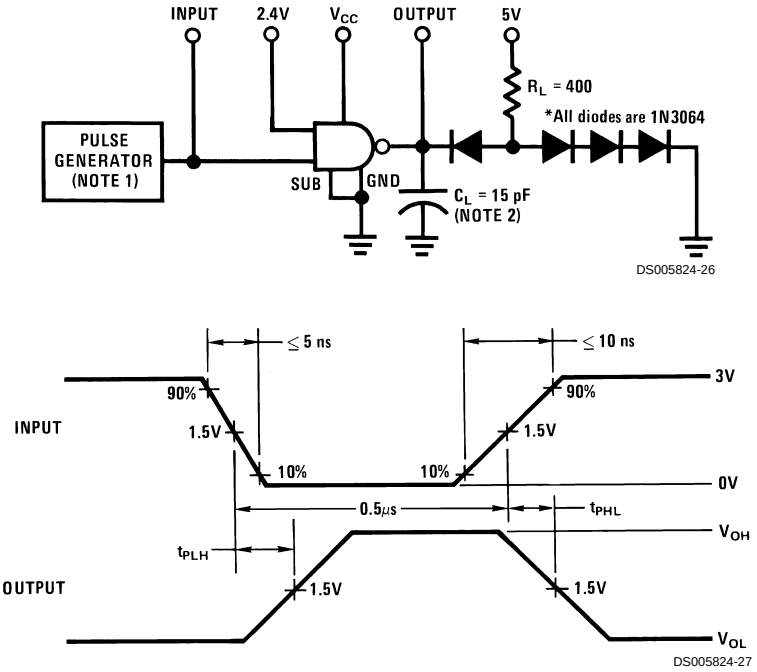
FIGURE 10. I_{CCH}, I_{CCL} for AND, NAND Circuits



Both gates are tested simultaneously.

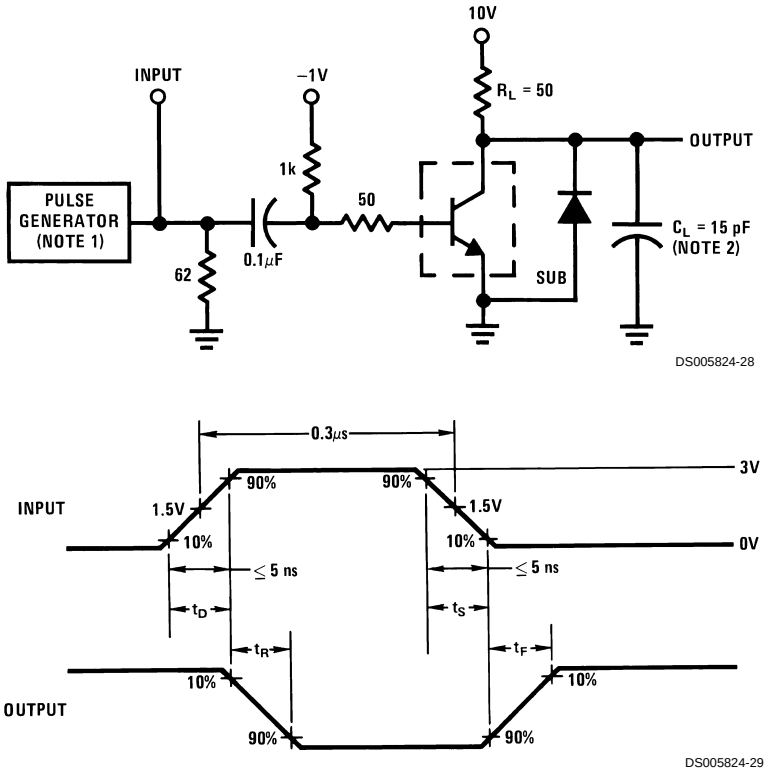
FIGURE 11. I_{CCH}, I_{CCL} for OR, NOR Circuits

AC Test Circuits and Switching Time Waveforms



Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

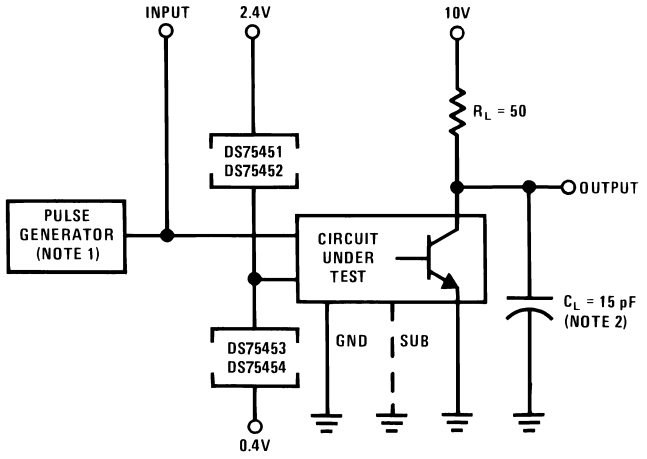
FIGURE 12. Propagation Delay Times, Each Gate

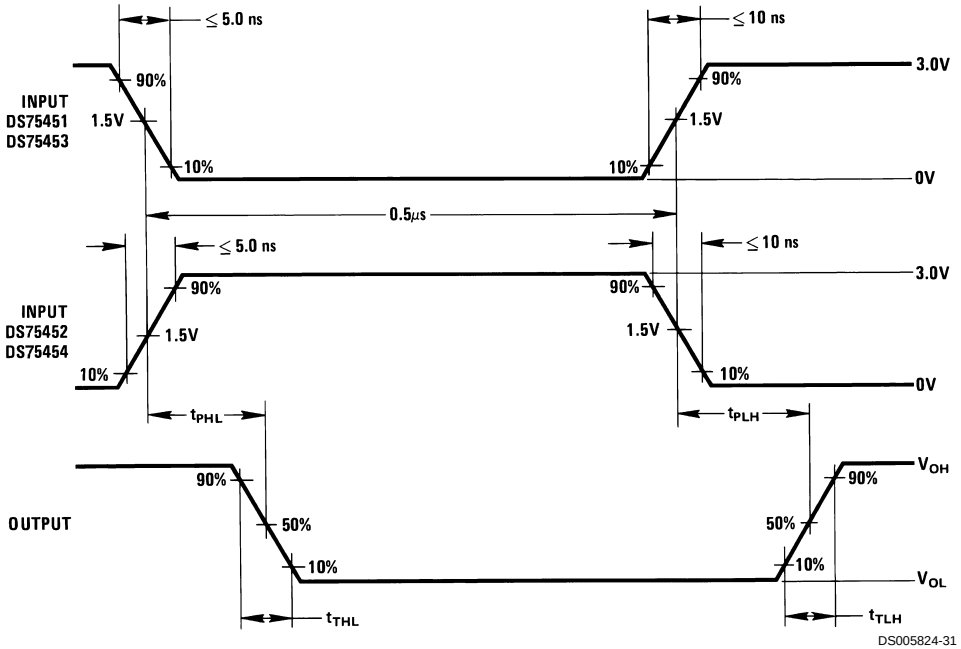


Note 1: The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

FIGURE 13. Switching Times, Each Transistor

AC Test Circuits and Switching Time Waveforms (Continued)

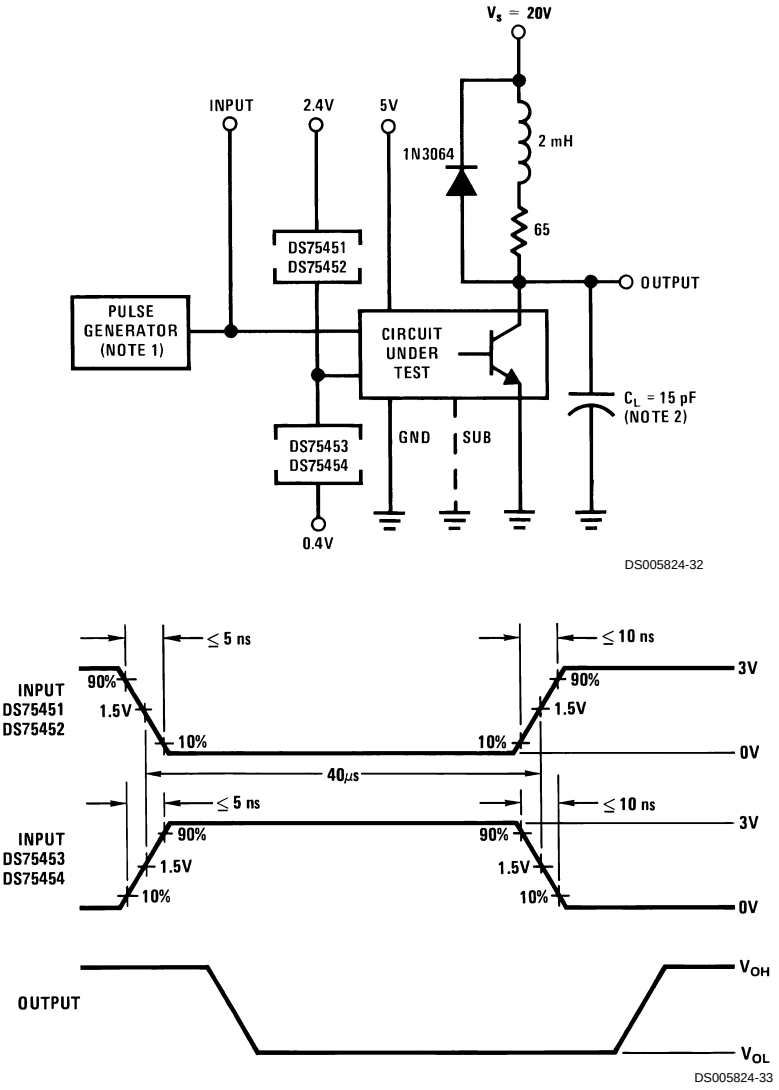




Note 1: The The pulse generator has the following characteristics: PRR = 1.0 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

FIGURE 14. Switching Times of Complete Drivers

AC Test Circuits and Switching Time Waveforms (Continued)



Note 1: The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

FIGURE 15. Latch-UP Test of Complete Drivers

Typical Performance Characteristics

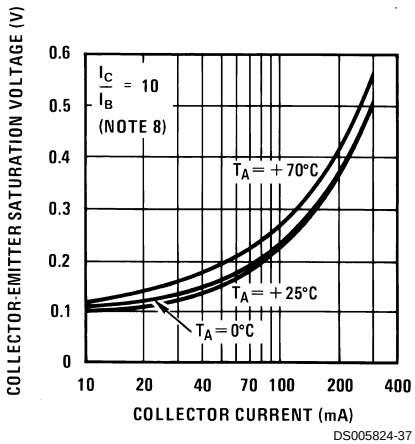
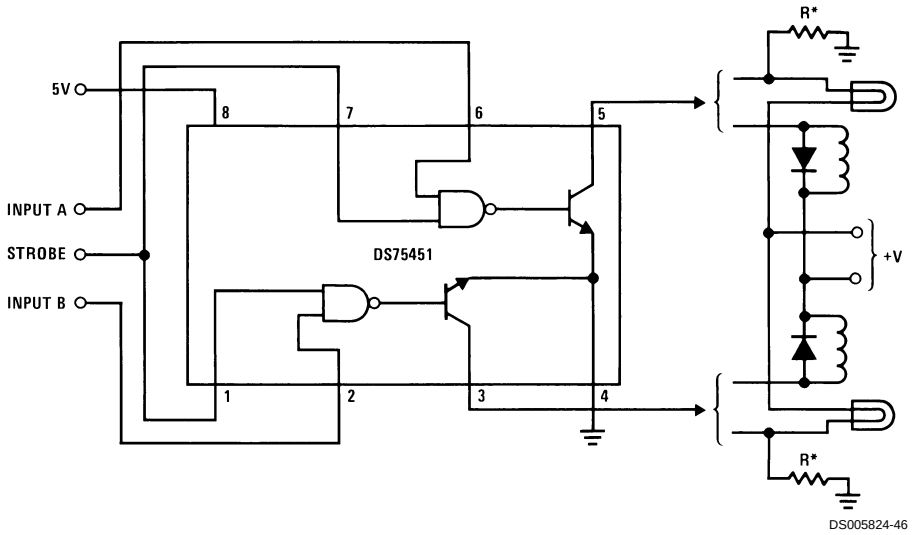


FIGURE 16. Transistor Collector-Emitter Saturation Voltage vs Collector Current

Typical Applications



*Optional keep-alive resistors maintain off-state lamp current at ≈ 10% to reduce surge current.

FIGURE 17. Dual Lamp or Relay Driver

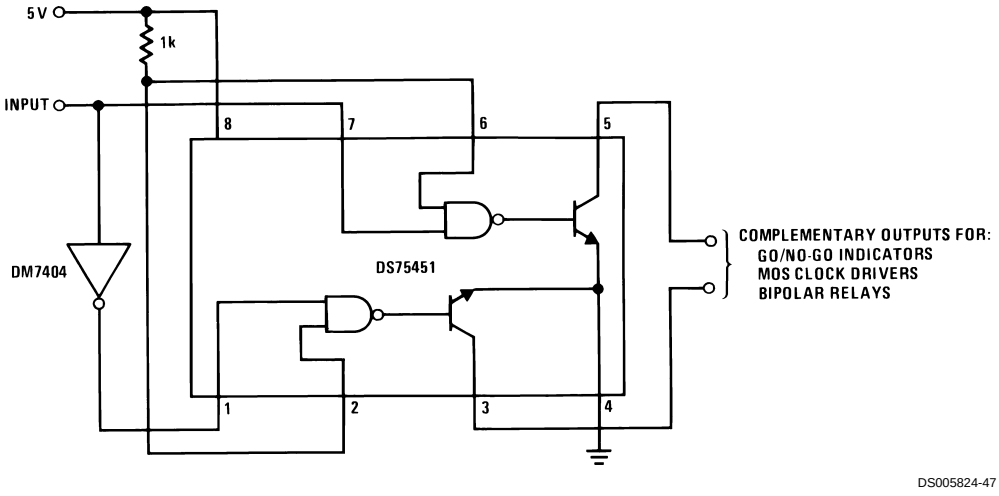


FIGURE 18. Complementary Driver

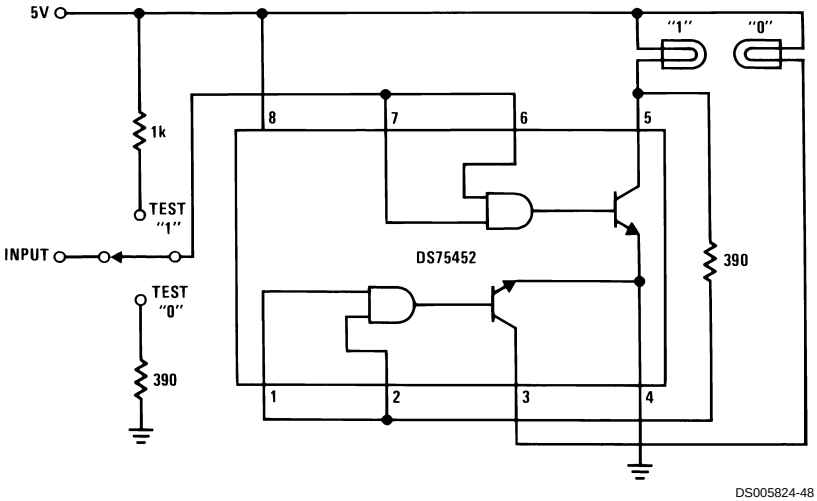
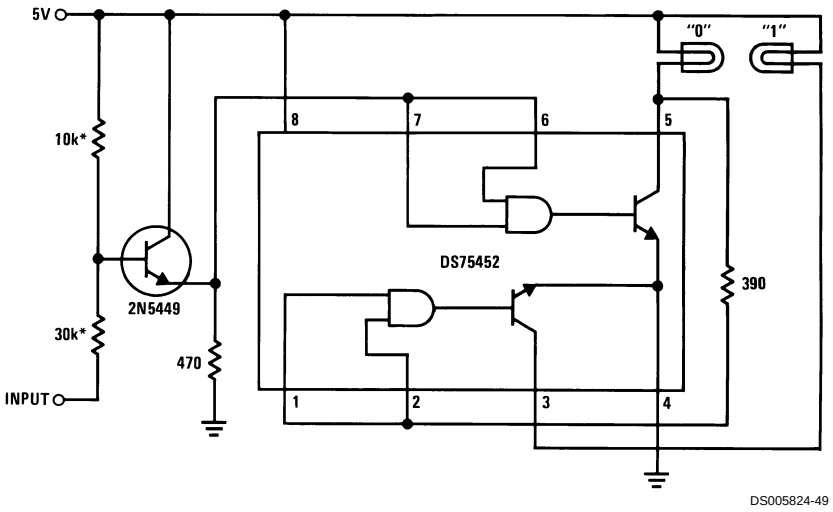


FIGURE 19. TTL or DTL Positive Logic-Level Detector

Typical Applications (Continued)



DS005824-49

*The two input resistors must be adjusted for the level of MOS input.

FIGURE 20. MOS Negative Logic-Level Detector

Typical Applications (Continued)

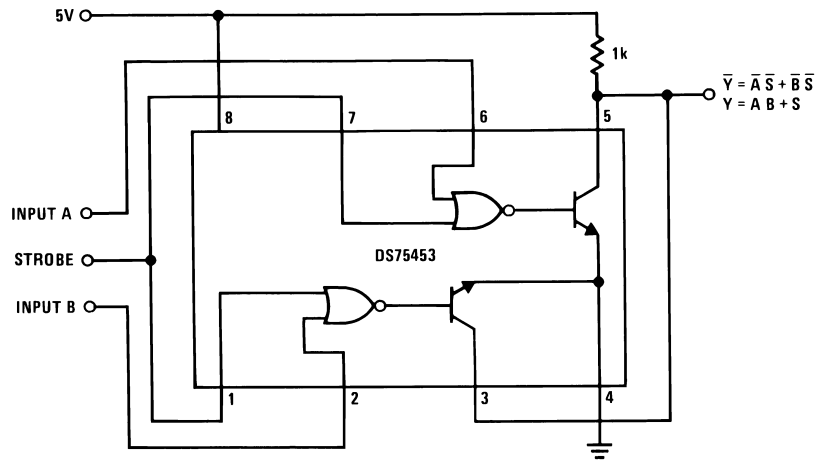
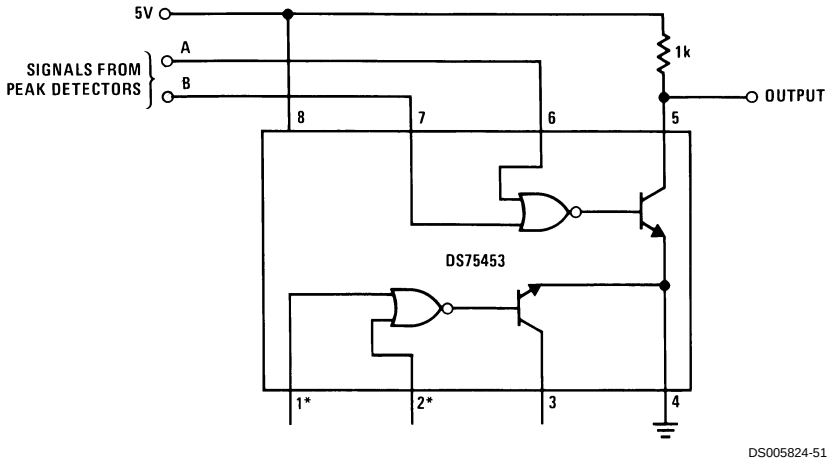
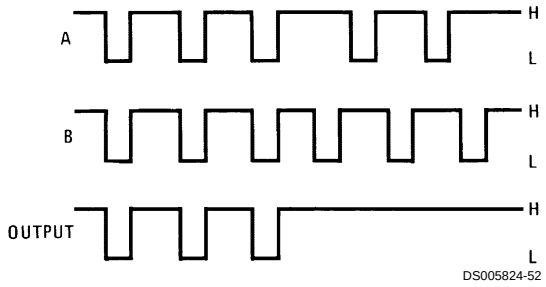


FIGURE 21. Logic Signal Comparator



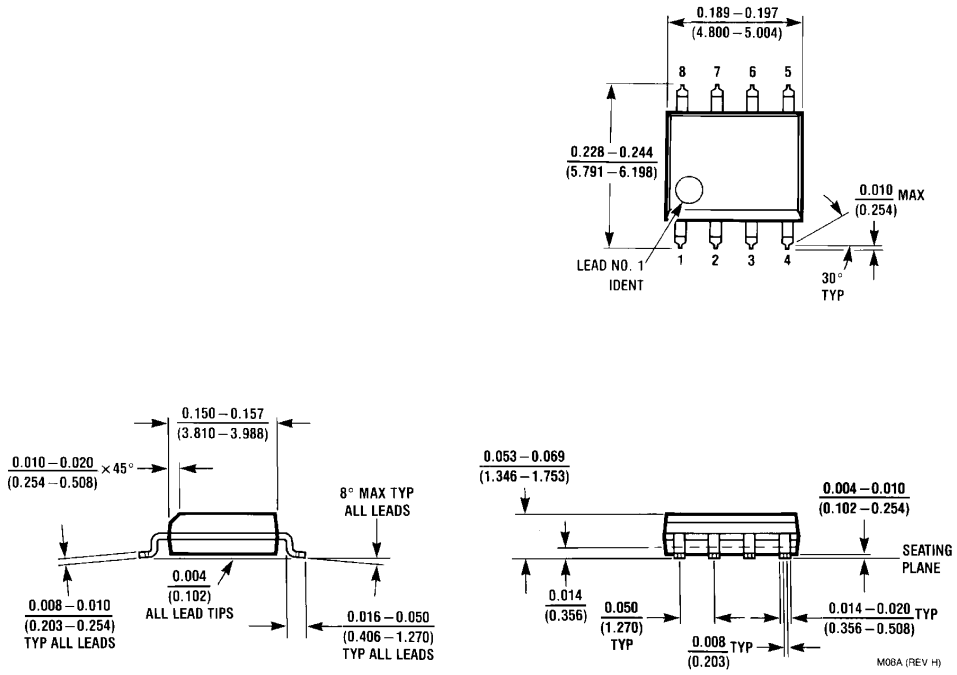
*If inputs are unused, they should be connected to +5V through a 1k resistor.



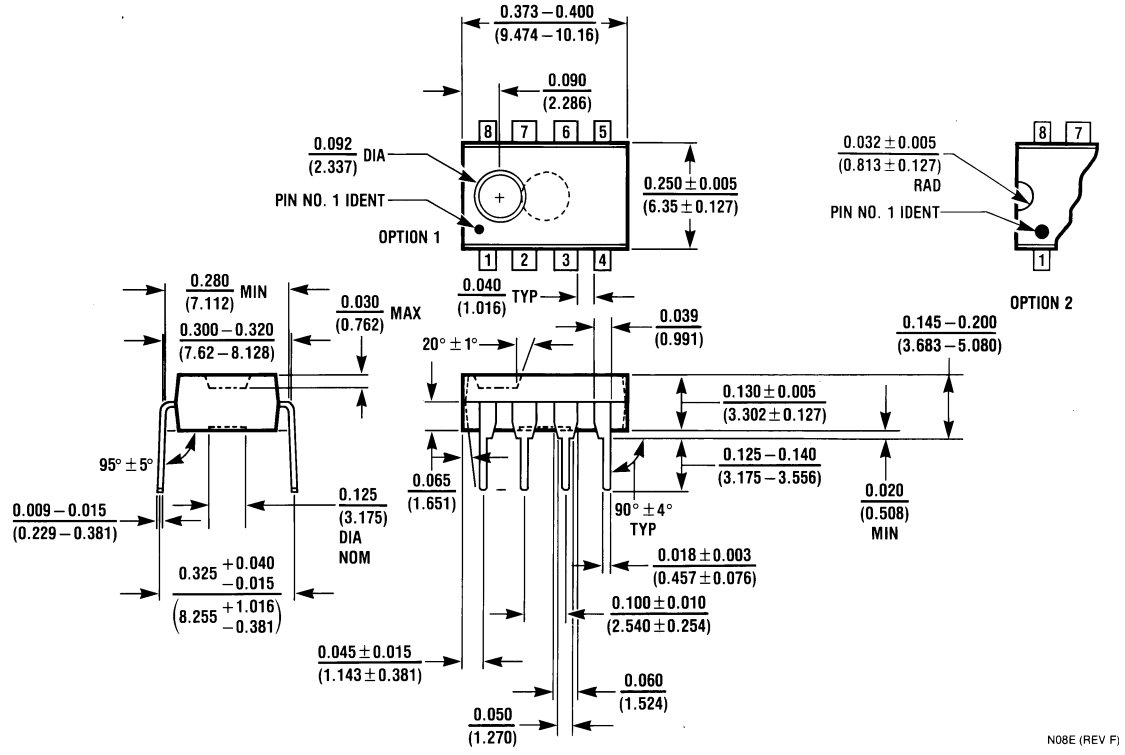
Low output occurs only when inputs are low simultaneously.

FIGURE 22. In-Phase Detector

Physical Dimensions inches (millimeters) unless otherwise noted



SO Package (M)
Order Number DS75451M, DS75452M, DS75453M
NS Package Number M08A



Molded Dual-In-Line Package (N)
Order Number DS75451N, DS75452N, DS75453N
NS Package Number N08E

Notes

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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